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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,756	08/25/2003	Shinji Endou	NECW 20.584	2786

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EXAMINER

HARRISON, CHANTE E

ART UNIT PAPER NUMBER

2677

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/647,756

Applicant(s)

ENDOU, SHINJI

Examiner

Chante Harrison

Art Unit

2677

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 8/26/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>8/03; 2/05 &amp; 7/05</u> | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Yasuyuki Kudo et al., US 20050200584 A1, 9/2005.

As per independent claim 1, Kudo discloses voltage generating means (fig. 3 "302") for generating reference voltages (Fig. 3 "316 & Gnd"), said voltage generating means having a plurality of resistors connected in series (Fig. 3 "307") between a first voltage power supply which supplies high-voltages (Fig. 3 "316") and a second power supply which supplies low-voltage (Fig. 3 "Gnd") and n reference voltage terminals (i.e. voltage terminals 321 to 330) (Fig. 3), which are more than said m gradation voltages (i.e. gray scale levels "315") (Fig. 3; pp. 4, Para 47), connected to respective junctions at which

Art Unit: 2677

said resistors are connected (i.e. selectors, SEL 308 to 313, connecting the resistor series to the gray scale levels of voltages) (Fig. 3); and voltage selecting means for selecting and outputting m red gradation voltages, m green gradation voltages, and m blue gradation voltages from the reference voltages supplied from said n reference voltage terminals (i.e. a control register has separate R, G and B adjustment registers storing set parameters for generating and selecting outputting a plurality of respective gradation voltages for each of R, G and B) (Fig. 9 "301"; Fig. 16 "1601 to 1603"; Fig. 15 "1505"; pp. 11, Para 107).

As per dependent claim 2, Kudo discloses said resistors of the voltage generating means have respective resistances set to the same value (i.e. resistors of voltage divider circuit in the resistor series have the same value) (Fig. 7A "1R"; pp. 8, Para 79).

As per dependent claim 3, Kudo discloses n reference voltage input lines extending in a first direction (i.e. resistors 321-330 extending vertically) (Fig. 3) and connected to said voltage generating means (i.e. voltage generating circuit 302) (Fig. 3); m red gradation voltage output lines (i.e. output gray scale levels generated by voltage divided resistors) (Fig. 3 "315"), m green gradation voltage output lines (i.e. output gray scale levels generated by voltage divided resistors) (Fig. 3 "315"), and m blue gradation voltage output lines (i.e. output gray scale levels generated by voltage divided resistors) (Fig. 3 "315"), all extending in a second direction perpendicular to said first direction (i.e. output lines for gray scale levels extend horizontally from the vertical resistor series) (Fig. 3

"315"); and connecting means disposed at points of intersection between lines in said first direction and lines in said second direction, for selectively connecting red gradation voltage output lines to one of the n reference voltage input lines, selectively connecting green gradation voltage output lines to one of said reference voltage input lines, and selectively connecting blue gradation voltage output lines to one of said reference voltage input lines (i.e. selectors connecting the resistors series to the lines for output gray scale levels for each of the respectively selected R, G and B adjustment registers that make separate gamma characteristic adjustments for R, G and B) (Fig. 3 "308 to 313"; Fig. 7A; Fig. 16 "1601 to 1603"; Fig. 15 "1505").

As per dependent claim 4, Kudo discloses connecting means comprises vias disposed at the points of intersection between the lines in said first direction and the lines in said second direction and interconnecting the lines in said first direction and the lines in said second direction (i.e. black dots at each resistor representing physical connection points between output voltage lines and the resistor series) (Fig. 7 "702").

As per dependent claim 5, Kudo discloses switches disposed at the points of intersection between the lines in said first direction and the lines in said second direction (i.e. SEL 308 to 313) (Fig. 3); and a switch control circuit (i.e. control register setting for micro adjustment register for each of R, G and B adjustment register) (Fig. 3 "306" connection to "308 to 313"; Fig. 16 "1601 to 1603") for selecting and rendering conductive one of n switches connected to each of said red gradation voltage output

lines (i.e. each R, G and B adjustment register separately makes gamma characteristic adjustments for respective R, G and B and each register has a micro adjustment register setting for controlling the switches that select the respective R, G or B gradation voltage output) (Fig. 7A "701, 704 to 706"), selecting and rendering conductive one of n switches connect to each of said green gradation voltage output lines (Fig. 7A "701, 704 to 706"), and selecting and rendering conductive one of n switches connected to each of said blue gradation voltage output lines (Fig. 7A "701, 704 to 706").

As per independent claim 6, Kudo discloses red, green and blue respective digital to analog converters each for selecting and outputting one of respective said m red, green or blue gradation voltages based on digital input data supplied thereto (i.e. the decoder is functionally equivalent to a digital to analog converter as it accepts input digital data respectively from R, G and B adjustment registers that each make separate gamma characteristic adjustments for R, G and B and outputs analog data to display) (Fig. 3 "303"; Fig. 16 "1601 to 1603"). The rationale as applied in the rejection of claim 1 applies herein.

As per dependent claim 7, Kudo discloses respective red, green and blue voltage selecting means (i.e. control register having R, G and B adjustment registers) (Fig. 16 "1601 to 1603") associated respectively with said red/green/blue digital to analog converters (i.e. the decoder is functionally equivalent to a digital to analog converter as it accepts input digital data respectively from R, G and B adjustment registers that each

Art Unit: 2677

make separate gamma characteristic adjustments for R, G and B and outputs analog data to display) (Fig. 3 "303"; Fig. 16 "1601 to 1603"), for supplying respective m red/green/blue gradation voltages selected from said n reference voltages (i.e. R, G and B adjustment registers that each make separate gamma characteristic adjustments for R, G and B outputs respective gray scale levels generated from reference voltages of the resistor series) (Fig. 3 "315").

### **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chante Harrison whose telephone number is 571-272-7659. The examiner can normally be reached on Monday, Tuesday and Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chante Harrison  
Examiner  
Art Unit 2677

Ch  
November 29, 2005

AMR A. AWAD  
PRIMARY EXAMINER  
